IN THE CLAIMS

Please amend the claims as follows, substituting any amended claim(s) for the corresponding pending claim(s):

1. (Withdrawn) A baseband controller system, comprising:
a plurality of buses coupled to communicate with a plurality of hardware blocks;
a microsequencer also coupled to the plurality of buses;
the microsequencer comprising a 72-bit correlator/ accumulator; and
transceiver circuitry coupled to at least one of the plurality of buses.

2. (Withdrawn) The baseband controller system of claim 1 wherein the microsequencer further comprises a 72-bit arithmetic logic unit.

3. (Withdrawn) The baseband controller system of claim 1 wherein the microsequencer further comprises a plurality of temporary registers for storing computational data.

4. (Withdrawn) The baseband controller system of claim 3 wherein the temporary registers include a 64-bit register.

5. (Withdrawn) The baseband controller system of claim 3 wherein the temporary registers include a 48-bit register.

6. (Withdrawn) The baseband controller system of claim 3 wherein the temporary registers include a 32-bit register.

7. (Withdrawn) The baseband controller system of claim 3 wherein the temporary registers include a 16-bit register.

8. (Withdrawn) The baseband controller system of claim 3 wherein the temporary registers include a 64-bit register, a 48-bit register, a 32-bit register and a 16-bit register.

9. (Withdrawn) The baseband controller system of claim 8 further including logic circuitry to determine which temporary register should be used to store a piece of computational data based upon the size of the piece of computational data.

10. (Withdrawn) The baseband controller system of claim 1 wherein the microsequencer comprises a plurality of clocks, including a native Bluetooth clock.

11. (Withdrawn) The baseband controller system of claim 1 wherein the microsequencer comprises a plurality of clocks, including a native real-time clock.

12. (Withdrawn) The baseband controller system of claim 1 wherein the microsequencer comprises a plurality of clocks, including an externally driven Bluetooth clock.

13. (Withdrawn) The baseband controller system of claim 1 wherein the microsequencer comprises a plurality of clocks, including an externally driven real-time clock.

14. (Withdrawn) The baseband controller system of claim 1 wherein the microsequencer comprises a plurality of timers.

15. (Withdrawn) The baseband controller system of claim 1 wherein the microsequencer comprises a plurality of timers wherein the plurality of timers comprises at least four timers.

16. (Withdrawn) The baseband controller system of claim 1 wherein the microsequencer includes eight timers.

17. (Currently Amended) A microsequencer for use as a real-time Bluetooth baseband controller~~, comprising~~ comprises:

timer circuitry operably coupled to receive a requested timer counting value and to announce when the timer counting value has elapsed;

temporary data storage circuitry operably coupled to store data; ~~and~~

a plurality of Bluetooth and native clocks operably coupled to support ~~for supporting~~ timing functionality of the timer circuitry according to Bluetooth specifications when in a master mode; and

a plurality of externally-driven Bluetooth and native clocks operably coupled to support timing functionality of the timer circuitry according to Bluetooth specifications when in a slave mode.

Claims 18 – 21 (Cancelled).

22. (Original) The microsequencer of claim 17 wherein the temporary data storage circuitry includes a 64-bit storage register.

23. (Original) The microsequencer of claim 17 wherein the temporary data storage circuitry includes a 48-bit storage register.

24. (Original) The microsequencer of claim 17 wherein the temporary data storage circuitry includes a 32-bit storage register.

25. (Original) The microsequencer of claim 17 wherein the temporary data storage circuitry includes a 16-bit storage register.

26. (Original) The microsequencer of claim 17 wherein the temporary data storage circuitry includes a 64-bit register, a 48-bit register, a 32-bit register and a 16-bit register.

27. (Currently Amended) The microsequencer of claim 17 wherein the temporary data storage circuitry ~~includes~~ comprises registers of different size and ~~further wherein the microsequencer includes~~ a data storage logic module, which data storage logic module determines which available register should be used for storing the data based upon the size of the data that is to be temporarily stored.

28. (Currently Amended) The microsequencer of claim 17 wherein the ~~timers include~~ timer circuitry comprises at least four timers.

29. (Currently Amended) The ~~micro-sequencer~~ microsequencer of claim 17 wherein the ~~timers include~~ timer circuitry comprises at least eight timers.

30. (Currently Amended) The ~~micro-sequencer~~ microsequencer of claim 27 further ~~including~~ comprises timer control logic circuitry for controlling the operation of the at least eight timers.

31. (Original) A microsequencer for use as a real-time Bluetooth baseband controller, comprising:

eight timers to provide traditional timer functionality;

timer control logic circuitry;

an externally driven Bluetooth clock;

an externally driven real-time clock;

a native Bluetooth clock;

a native real-time clock;

a 64-bit register for temporarily storing computational data;

a 48-bit storage register for temporarily storing computational data;

a 32-bit storage register for temporarily storing computational data;

a 16-bit storage register for temporarily storing computational data; and

data storage logic circuitry for determining which of the temporary storage registers is to store a piece of data that is to be temporarily stored.

32. (Original) The microsequencer of claim 31 wherein the period of one Bluetooth clock cycle is equal to 312.5 real-time clock cycle periods.